

MM23SC4428
1-KByte EEPROM with
write protect function
and PSC

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1-KBYTE EEPROM WITH WRITE PROTECT FUNCTION AND PROGRAMMABLE SECURITY CODE (PSC)

FEATURES

- Standard CMOS process
- 1024 X 8 bits EEPROM organization
- Byte-wise addressing
- Byte-wise erase/write
- Irreversible byte-wise write protection
- Single 5V power supply for read and write/erase
- Low power operation:
3 mA typical active current
- 5 ms programming time
- 3-wire serial interface
- 20 KHz serial clock rate
- Contact configuration and serial interface, ISO standard 7816 (Synchronous Transmission) compatible
- High ESD protection : > 4 KV
- High reliability :
 - 500,000 erase/write cycles guaranteed
 - Typical 1 million erase/write cycles
 - 10 years data retention
- Wide operating temperature range, 0 to +70 °C
- 2-byte Programmable Security Code (PSC) for write/erase protection

DESCRIPTION

MM23SC4428 contains 1024 x 8 bits of EEPROM with programmable write protection for each byte. Random read access to any byte in the memory is always possible. The memory can also be erased and written byte by byte. Erasing old data in the byte location must be performed before new data can be written to the new location. Each byte in the memory has a corresponding protect bit. The protect bits are only one time programmable and cannot be erased. After the protect bits are enabled (logic 0), the corresponding bytes can never be changed again. A write-protect bit with data-compare function is available for user to verify the data in the memory before enabling the protect bit.

MM23SC4428 also offers two bytes of Programmable Security Code (PSC) against unauthorized memory write/erase operations. All the memory, except for the PSC can always be read, but the memory can be written or erased only after PSC verification. If the user fails to enter the correct PSC in eight consecutive attempts, the device will block any further PSC entry attempts and the memory can never be erased or written again.

The PSC bytes are pre-programmed by the manufacturer with a code, which is specified for customer for device transport security purposes, before the device are shipped to the customer. The Error Counter will be pre-erased by the manufacturer to allow maximum attempts (maximum of eight) for PSC entry.

BLOCK DIAGRAM

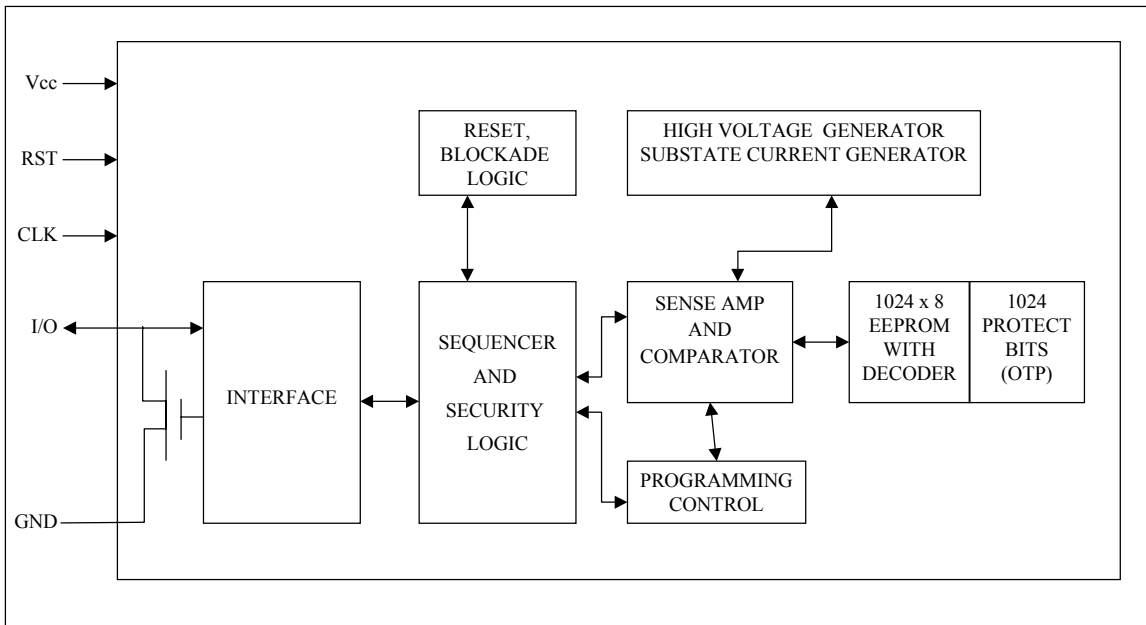


Figure 1 : Block Diagram

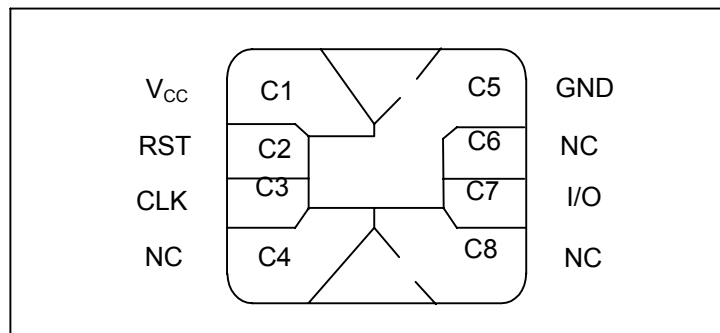


Figure 2: Pin Configuration – Smartcard contact for M2

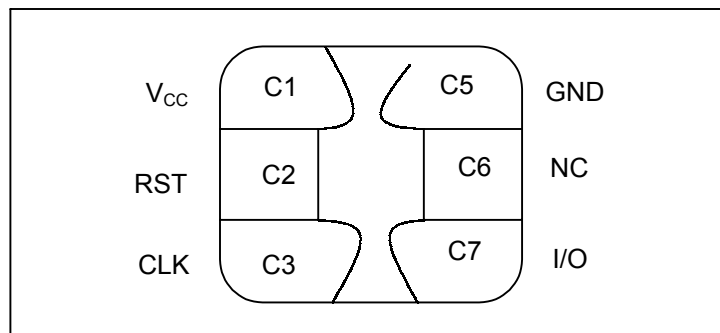


Figure 2a: Pin Configuration – Smartcard contact for M3

PIN NAMES AND DESCRIPTIONS

Pin	Card Contact (M2)	Symbol	
1	C1	Vcc	Supply Voltage
2	C2	RST	<p>Reset: The device reset pin is used to take the device out of the power on reset state (POR). When the operating power is first applied to Vcc, the device goes into POR state. The POR state can be terminated by the RST in this sequence: bring RST from 0 to 1 and then change CLK from 0 to 1 (See Figure 3). This reset operations terminates any active command operation. After POR state has been terminated, an Answer to Reset (ATR) operation must be performed before any data can be erased or written.</p> <p>This device also comply with ISO7816 specification on Answer to Reset function. The Answer to Reset can be invoked by performing the following steps;</p> <ol style="list-style-type: none"> 1. RST goes from 0 to 1 2. CLK pulse is applied 3. RST changes from 1 to 0 <p>If these steps are performed correctly, the device will set the address counter to 0 and the first data bit at byte address 0 will appear on the output (I/O). By continuing to send pulses at CLK, the contents of the following byte addresses can be read out of the device.</p> <p>In normal operation, RST controls the data input and output directions. When sending data/command to the device, RST is set to 1. When reading data/PSC verification output from the device, RST is set to 0.</p>
3	C3	CLK	Serial Clock : This is the device data clock pin. It is used to clock data bits into and out of the device.
4	C4	NC	No Connection
5	C5	GND	Ground
6	C6	NC	No Connection
7	C7	I/O	Serial Data I/O (open drain) : This pin is where data is shifted in and out of the device.
8	C8	NC	No Connection

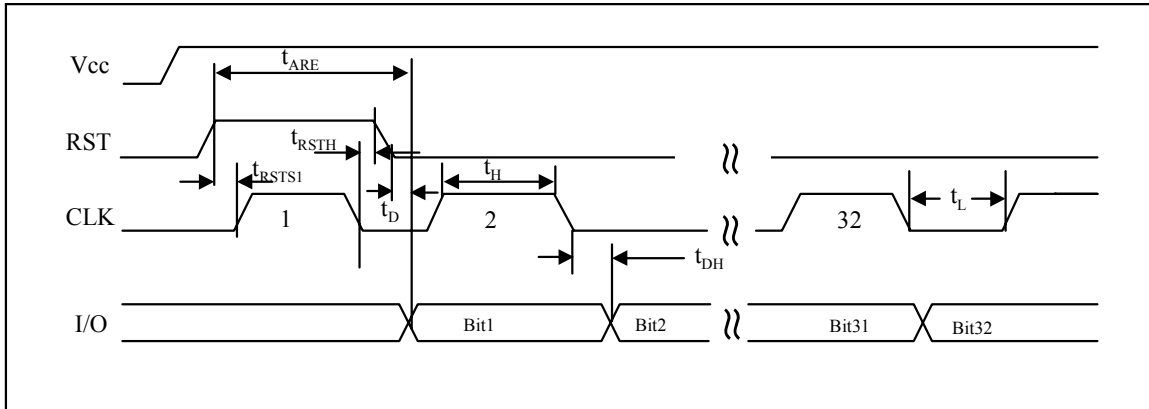


Figure 3 : Reset and Answer to Reset Timing Diagram

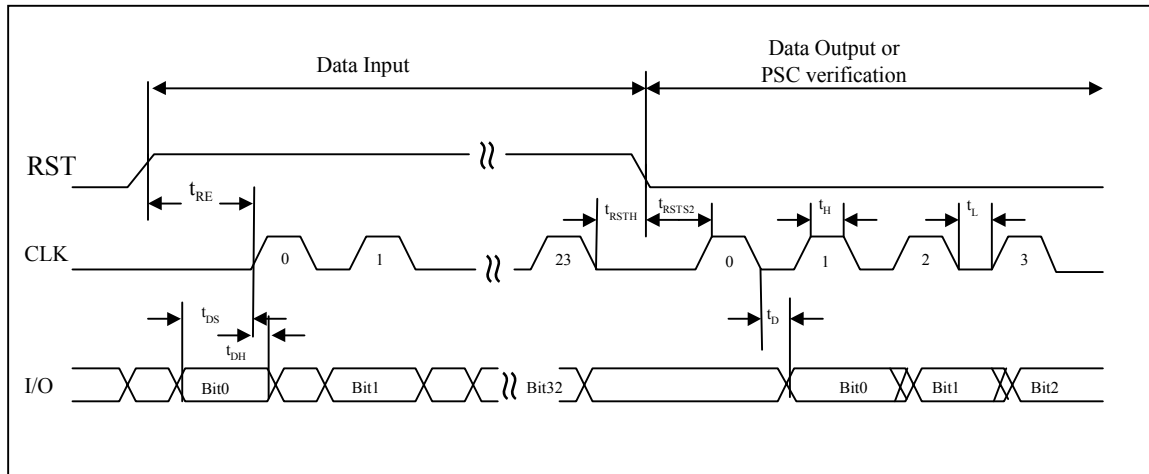


Figure 4 :General Timing for Data Input, Data Output and PSC Verification

Table 1 : Control Words for MM23SC4428

Command Name	Byte 1								Byte 2	Byte 3
	S0	S1	S2	S3	S4	S5	A8	A9	A0 – A7	D0–D7
Read 8 bits data without protect bit	0	1	1	1	0	0	Address bit 8 and 9		Address bit 0 - 7	Don't Care
Read 9 bits data with protect bit	0	0	1	1	0	0				Don't Care
Write and erase without protect bit ^{(1),(2)}	1	1	0	0	1	1				Input Data
Write and erase with protect bit ^{(1),(2)}	1	0	0	0	1	1				Input Data
Write protect bit with data comparison ⁽¹⁾	0	0	0	0	1	1				Compare Data
Write Error Counter	0	1	0	0	1	1	1	1	FDH	Bit Mask
Verify first PSC byte	1	0	1	1	0	0	1	1	FEH	PSC byte 1
Verify second PSC byte	1	0	1	1	0	0	1	1	FFH	PSC byte 2

Notes:

- (1) If the protect bit of the byte is enable, the write command will have no effect on the byte content.
- (2) Locations 1021 – 1023 are occupied by Error Counter and PSC byte and thus cannot be used for general data storage.

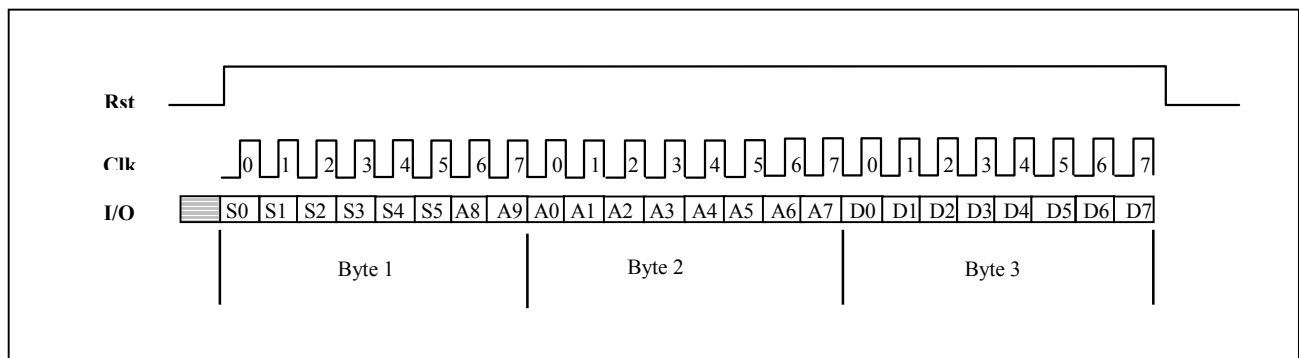


Figure 3 :Command Entry Sequence

GENERAL COMMAND DESCRIPTIONS

Read 8-bit Data

The read 8-bit data command allows the user to specify the address (A0-A9) of the data byte to be read from the devices. The byte address for the next output data is automatically incremented after every eight-clock pulse. The data is output in sequential order, with the data from address n followed by the data from address n+1. (See Figure. 6)

Read 9-bit data with Protect Bit

The read 9-bit data command operates similarly to read 8-bit data command excepts that the protect bit for each byte is output after each 8-bit data and the address for the next output data is incremented after every nine clock pulses. (See Figure 7).

Write/Erase Data Byte without Protect Bit

The Write/Erase data byte without protect bit command writes the new data into the specified byte location. There are three kind of Write/Erase operations which are automatically executed by the devices:

1. Erase and subsequent write if 203 clock pulses at $f < 20\text{KHz}$ are applied. (See Figure 8).
2. Write only if 103 clock pulses at $f < 20\text{KHz}$ are applied. This operation is only suitable if single bit of one byte shall be change only from 1 to 0. (See Figure. 9)

3. Erase only if the input data = FFH and 103 clock pulse at $f < 20\text{KHz}$ are applied. (See Figure. 9).

If the protect bit of the corresponding byte location is enabled, the write/erase operations will have no effects on the content.

Write/Erase Data Byte with Protect Bit

The Write/Erase data byte with protect bit command operates similarly to the write/erase data byte with protect bit command except that it also writes 0 to the corresponding protect bit. After the protect bit is set to 0 (write protection enabled), it cannot be changed again. (See Figure. 8 and 9).

Write Protect Bit with Data Comparison

The write protect bit with data comparison command writes 0 to the corresponding protect bit only if the input data and the data in the specified memory location are the same. After the protect bit is set to 0 (write protection is enabled), it cannot be changed again. (See Figure. 9).

The execution of write/erase command are terminated after a given number of clock cycles. When the operation is done, the devices will bring the I/O states to 0. Only RST transition from 0 to 1 can set the I/O state back to 1.

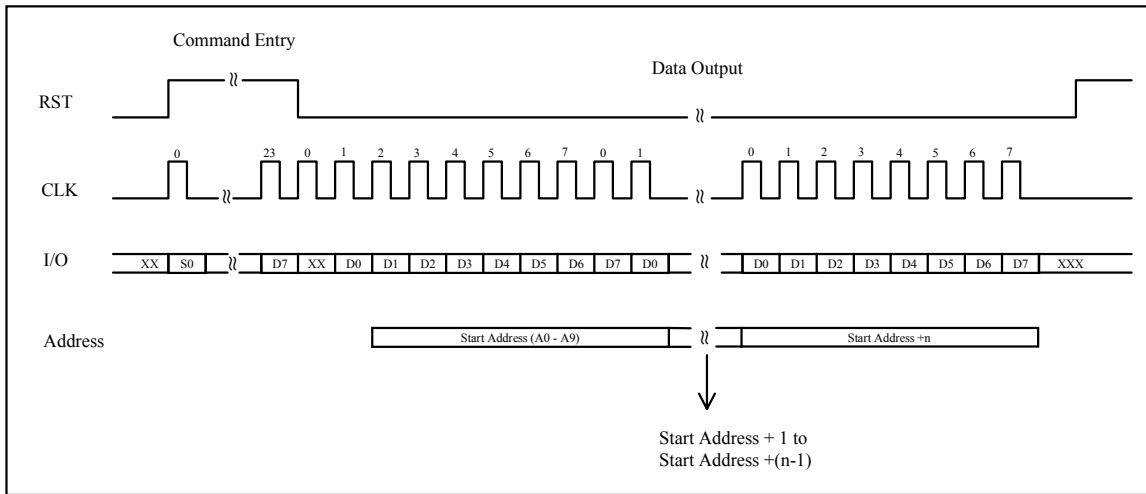


Figure 6 : Read 8-bit Data

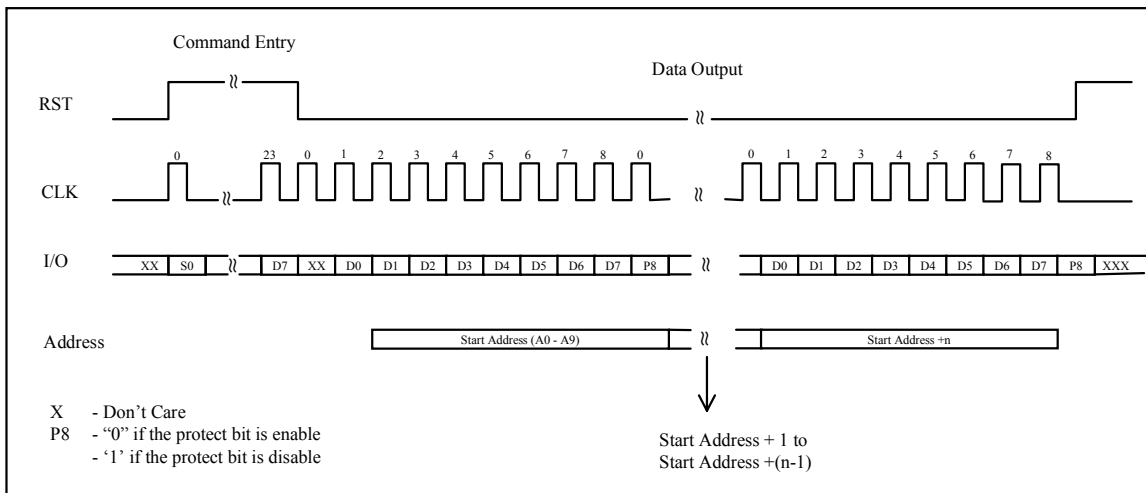


Figure 7 :Read 9-bit Data with Protect Bit

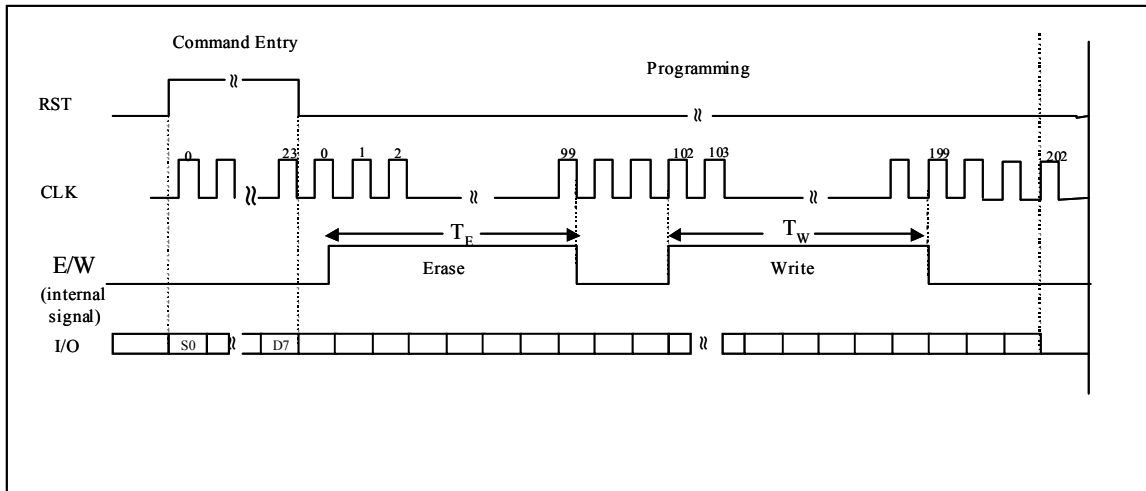


Figure 8: Programming Erase and Write

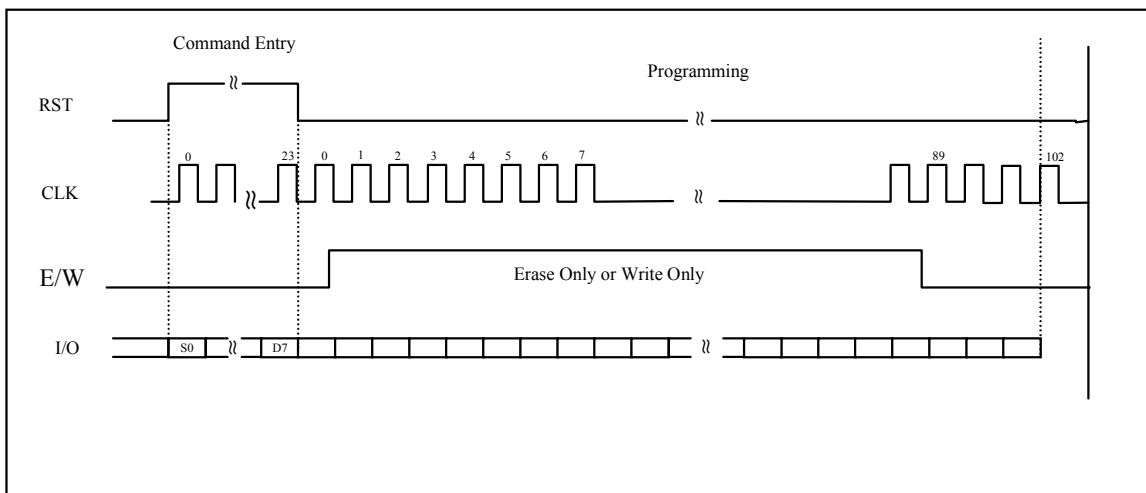


Figure 9: Programming Erase Only or Write Only

SECURITY FEATURES

Overview

Without entering the Programmable Security Code, only memory read access is possible. However, the content of the PSC addresses (1022 and 1023) cannot be read out. If reading PSC is attempted, 00H will be output. The PSC verification procedure must be performed by the following sequence :

1. Write one not-written Error Counter bit, address 1021
2. Enter first PSC byte, address 1022
3. Enter second PSC byte, address 1023
4. After successful PSC verification, the Error Counter should be erased to reactivate the 8 PSC entry attempts. If

the PSC entry incorrect, go back to step 1. If all the Error Counter bits have been written, any further PSC entry will be blocked and the memory can never be changed again.

Writing Error Counter

The number of erased bit (logic 1) in Error Counter determines the number of possible attempts (maximum of 8). After PSC is successfully verified, the counter can now be erased. Before disconnecting the supply voltage Vcc, the counter should be erased in order to reactivate the eight attempts.

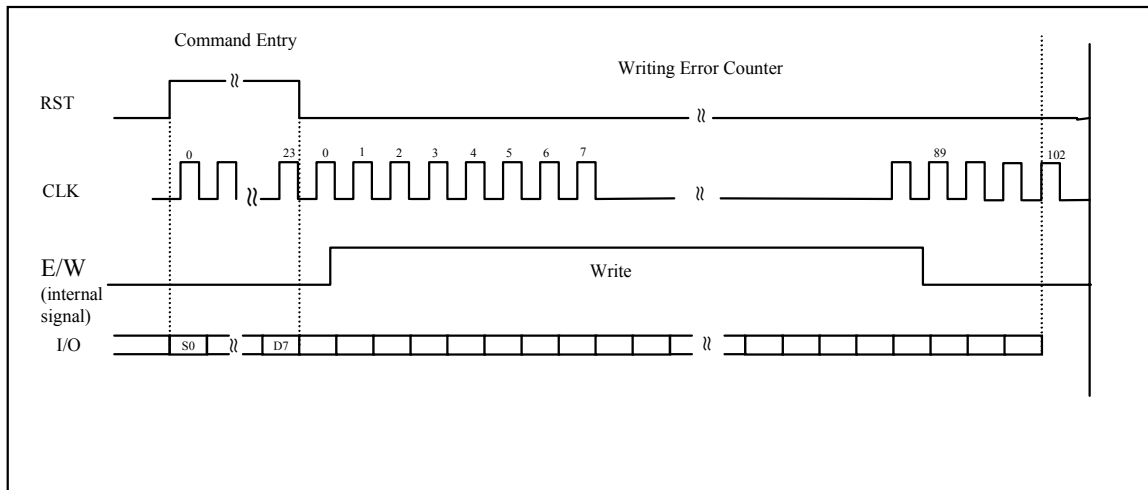


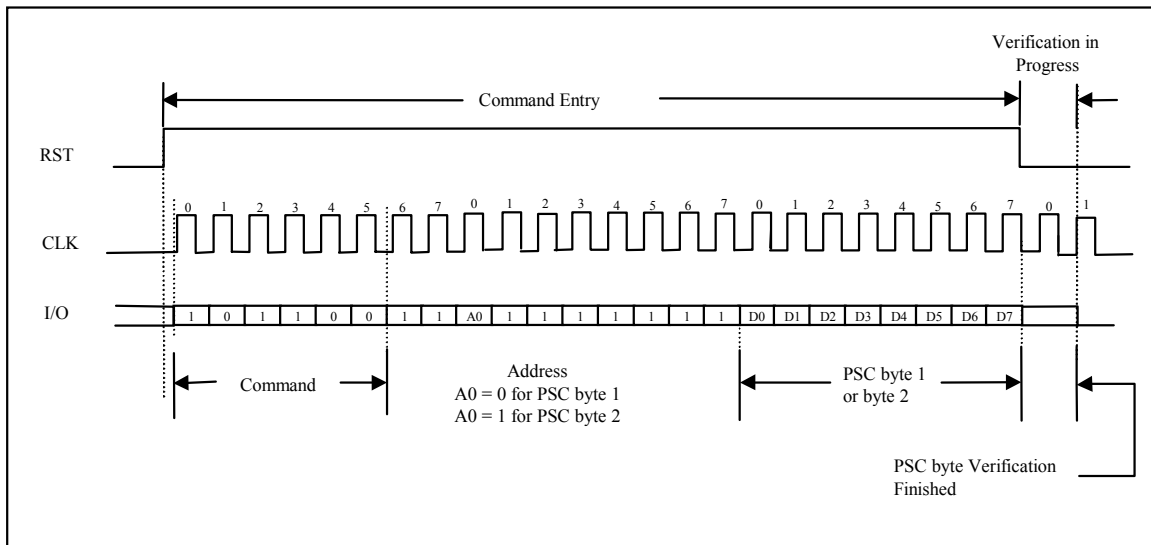
Figure 10 :Writing Error Counter

Entry of PSC

The least significant PSC byte beginning with the least significant bit must be entered first and then the most significant. If both PSC byte 1's and byte 2's comparisons

prove correct, the memory erase/write access will be enable and PSC may changed as wished, except the corresponding protect bits are 0 (enable).

Figure 11 :PSC Verification



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	- 0.3	6	V
V _I	Input Voltage	- 0.3	6	V
T _{STG}	Storage Temperature	- 40	125	° C
P _{MAX}	Power Dissipation	-	60	MW

CAPACITANCE (T_A = 25°C, V_{CC} = 5.0 ± 10%, f = 1 MHz)

Symbol	Parameter	Conditions	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	pF

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{CC}	Supply Voltage		4.5	5.0	5.5	V
I _{CC}	Supply Current		-	3	10	mA
V _{IH}	Input HIGH Voltage (I/O, CLK, RST)		3.5	-	5.0	V
V _{IL}	Input LOW Voltage (I/O, CLK, RST)		0	-	0.8	V
I _{IH}	Input HIGH Current (I/O, CLK, RST)		-	-	10	µA
I _{OL}	Output LOW Current	V _{OL} =0.4V open drain	0.5	-	-	mA
I _{OH}	Output HIGH Leakage Current	V _{OH} =5V open drain	-	-	10	µA

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
f _C	Clock Frequency		-	20	-	KHz
t _{RE}	Reset Time		9	-	-	µs
t _{ARE}	Answer to Reset		20	50	-	µs
t _H	Clock HIGH Period		10	-	-	µs
t _L	Clock LOW Period		10	-	-	µs
t _W	Write Time	(f _c = 20 KHz)	5	-	-	ms
t _E	Erase Time	(f _c = 20 KHz)	5	-	-	ms
t _{RSTS1}	Reset Setup Time 1		4	-	-	µs
t _{RSTS2}	Reset Setup Time 2		4	-	-	µs
t _{DS}	Write Data Setup Time		4	-	-	µs
t _{DH}	Write Data Hold Time		4	-	-	µs
t _D	Read Data Delay Time		6	-	-	µs
t _R	Rise Time (I/O, CLK, RST)		-	-	1	µs
t _F	Fall Time (I/O, CLK, RST)		-	-	1	µs

ORDERING INFORMATION**Temperature Range: 0° to +70°C**

Order Part Number	Package
MM23SC 4428 - SW	Sorted wafer (standard wafer)
MM23SC 4428 - SN	Sawn wafer (on a ring after backgrinding to 7 mil or specified)
MM23SC 4428 - DW	Die in waffle pack (after backgrinding and saw)
MM23SC 4428 - M2	On a module M2 - 8 pins
MM23SC 4428 - M3	On a module M3 - 6 pins

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